PWM Current Mode Controller with Quasi-Resonant Operation

REV：00

General Description

The LD7580A is a current mode PWM controller and features quasi resonant operation. It operates in DCM at light load to optimize the efficiency and operates in boundary condition at high power level.

The LD7580A is integrated with high voltage startup circuit, green-mode power-saving operation, and leading-edge blanking of the current sensing. It also incorporates with several protections like OLP (Over Load Protection), OVP (Over Voltage Protection), OTP (Over Temperature Protection) …etc. Highly integration and tiny package make it an ideal choice in wide variety of applications, and in addition to minimize the component counts and the circuit space.

In capable of performing boundary operation, it can reduce the switching loss and the reverses recovery loss of rectify diode when the MOSFET turns on. It is designed to meet the latest power saving regulations for wide input voltage range of applications.

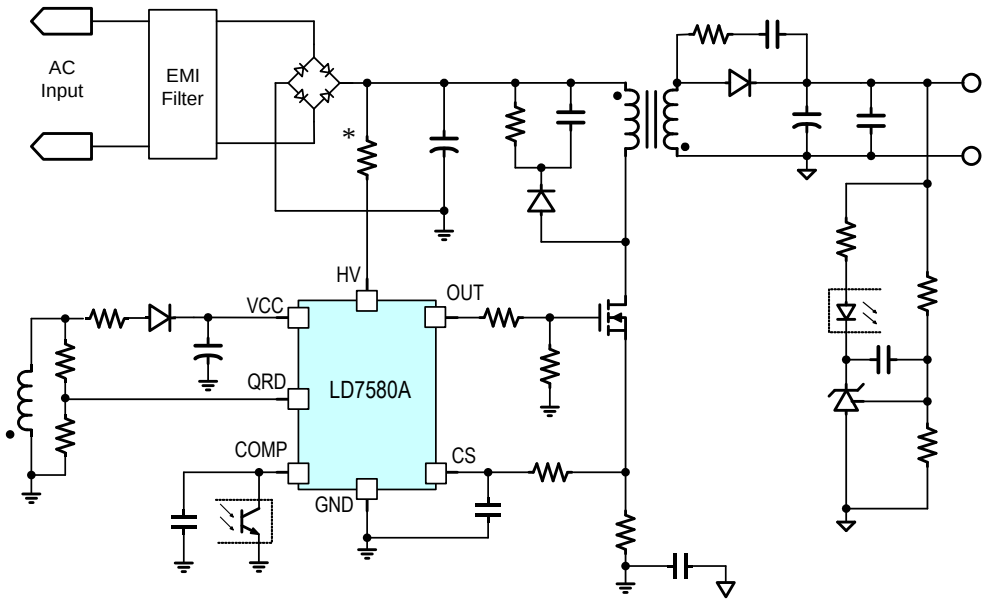
Features

- High-Voltage (500V) Startup Circuit
- Current Mode Control
- Minimum Drain Voltage Switching
- Green Mode Control at Light Load
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Over Voltage Comparator on VCC and QRD Pin
- OLP (Over Load Protection)
- Internal Over Temperature Shutdown
- +500/-700mA Driving Capability

Applications

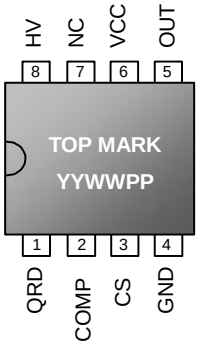
- Switching AC/DC Adaptor
- Open Frame Switching Power Supply
- LCD Monitor/TV Power Supply

Typical Application



Pin Configuration

SOP-8 & DIP-8 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

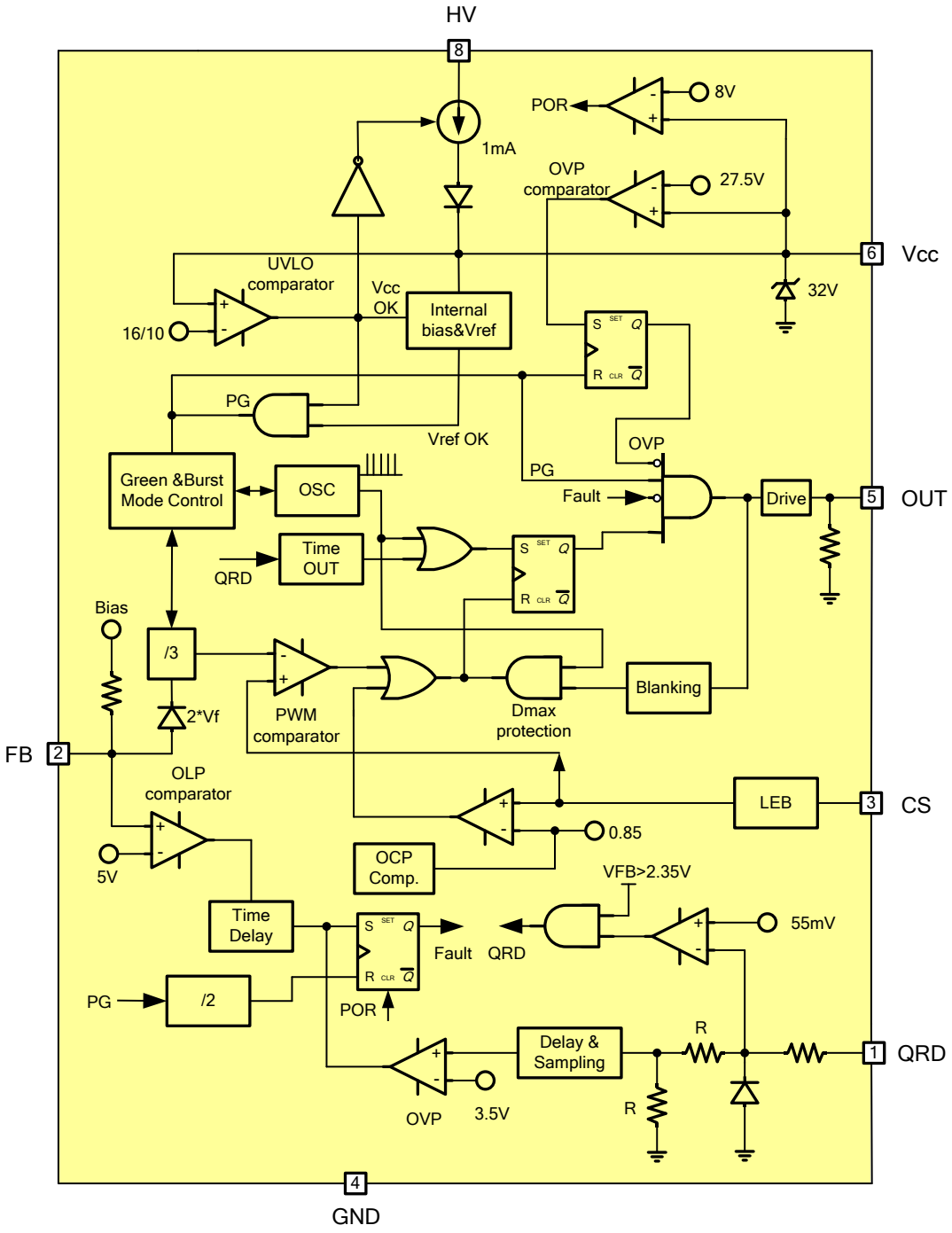
Part number	QRD-OVP protection	Protection Mode OLP/ Vcc OVP	Package	Top Mark	Shipping
LD7580AGS	Yes	Auto-recovery	SOP-8	LD7580AGS	2500 /tape & reel
LD7580AGN	Yes	Auto- recovery	DIP-8	LD7580AGN	3600 /tube /Carton

The LD7580A is RoHs Compliant/ Green Packaged.

Pin Descriptions

PIN	NAME	FUNCTION
1	QRD	Quasi Resonant detection. A voltage signal will be issued from the auxiliary winding after the transformer's core is completely demagnetized. The auxiliary winding voltage will decrease until it reaches the internal setting value, and then enter QR mode operation. In addition, an over voltage comparator (with 3.5V reference voltage) is built-in with QRD pin. Once OVP is detected, the LD7580A will turn off immediately.
2	COMP	Voltage feedback pin (same as the COMP pin in UC384X). Connect a photo-coupler to close the control loop and achieve the regulation. Voltage of COMP pin varies in proportion to output power. This pin also provide over load protection function, if the voltage of COMP pin higher than a threshold of around 5.0V and more than 60ms, the controller will stop OUT signal and enter protection mode.
3	CS	Current sense pin. Primary side current is sensed and determined for its max level through a resister. The sensed signal will be compared with DC voltage (0.85V Typ.) across LEB circuit. Primary current is limited by OCP comparator cycle by cycle.
4	GND	Ground. Connect a capacitor between VCC and GND.
5	OUT	Gate drive output, to drive the external MOSFET.
6	VCC	Supply voltage pin. Connect a 0.1μF bypass capacitor between VCC and GND pins as close as possible to filter high frequency noise. With the high voltage start-up circuit, a start-up resister is eliminable.
7	NC	Unconnected pin to ensure adequate creep age distance
8	HV	Connect this pin to positive terminal of bulk capacitor to provide 1mA to VCC bulk capacitor through constant current source. When Vcc voltage trips the UVLO (on), this HV loop will be turned off to reduce the power loss of startup circuit. A current limit resistor is strongly recommended to be placed between high voltage side and HV pin to avoid negative turn-on spike.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V~30V
High-Voltage Pin, HV	-0.3V~500V
FB, CS, QRD	-0.3V~7V
OUT	-0.3V~Vcc+0.3V
Maximum Junction Temperature	150°C
Operating Ambient Temperature Range	-40°C to 85°C
Operating Junction Temperature Range	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8)	160°C/W
Package Thermal Resistance (DIP-8)	100°C/W
Power Dissipation (SOP-8, at Ambient Temperature = 85°C)	250mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	400mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (Except HV Pin)	2.5KV
ESD Voltage Protection, Human Body Model (HV Pin)	1.0KV
ESD Voltage Protection, Machine Model (Including HV Pin)	250V
Gate Output Current	+500/-700mA

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Supply Voltage Vcc	12	26	V
COMP Capacitor Value	1	100	nF

Note:

1. It's essential to connect a capacitor to COMP pin to filter out the undesired switching noise for stable operation.
2. The small signal components should be placed around the IC pin as close as possible.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High-Voltage Supply (HV Pin)					
High-Voltage Current Source	V_{CC}< UVLO(on),HV=500V	0.5	1.0	1.5	mA
Off-State Leakage Current	V_{CC}> UVLO(off) ,HV=500V	0	-	35	μA
Supply Voltage (VCC Pin)					
Startup Current		-	300	390	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V	-	2.5	3.5	mA
	V_{COMP}=3V	-	2.5	3.5	mA
	OLP tripped	-	0.5	0.8	mA
	OVP tripped (Vcc pin/ QRD pin)	-	0.6	0.8	mA
	Internal OTP tripped	-	0.5	0.8	mA
UVLO (OFF)		9	10	11	V
UVLO (ON)		15	16	17	V
OVP Level		27	28	29	V
Voltage Feedback (COMP Pin)					
Short Circuit Current	V_{COMP}=0V	1.1	1.5	2.4	mA
Open Loop Voltage	COMP pin open	5.2	5.8	6.6	V
Burst Mode Trip Level		-	1.4	1.6	V
Green Mode Threshold Vcomp		-	1.75	-	V
QR Mode ON Threshold		-	2.35	2.6	V
QR Mode Hysteresis		-	0.25	0.35	V
QR Mode Blanking Time		6.2	8	9.8	μS
QR Mode Time Out		-	29	35	μS
Current Sensing (CS Pin)					
Maximum Input Voltage, Vcs(off)		0.80	0.85	0.90	V
Leading Edge Blanking Time		-	200	320	nS
Input impedance		1	-	-	MΩ
Delay to Output		-	100	150	nS

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator for Switching Frequency					
Green Mode Frequency		-	20	-	KHz
Maximum ON Duty, D_{MAX}	V_{FB}<OLP trip level	-	75	80	%
Temp. Stability	T_A= -20°C ~85°C	0	5	-	%
Voltage Stability	VCC=11V-25V	0	1	-	%
QRD (Quasi Resonant Detection)					
I_{QR}(flow into QRD pin)		-	1	2	μA
Input Impedance			28	34	KΩ
QRD Threshold Voltage		28	55	82	mV
QRD Threshold Hysteresis		-	25	-	mV
QRD Delay Time		180	250	350	nS
Sampling OVP Trip Level		6.2	7	7.5	V
OVP Delay Time		-	1.6	2.5	μS
OVP Sampling Time		-	0.8	2	μS
OVP De-latched Level (VCC Pin)		9	10	11	V
Gate Drive Output (OUT Pin)					
Output Low Level	VCC=15V, Io=20mA	-	-	1	V
Output High Level	VCC=15V, Io=20mA	8	-	-	V
Rising Time	Load Capacitance=1000pF	-	60	200	nS
Falling Time	Load Capacitance=1000pF	-	30	100	nS
OLP (Over Load Protection)					
OLP Trip Level	COMP pin Open	4.5	5.0	5.5	V
OLP Delay Time		-	60	75	mS
OTP (Over Temperature)					
OTP Level		-	140	-	°C
OTP Hysteresis		-	15	-	°C

Typical Performance Characteristics

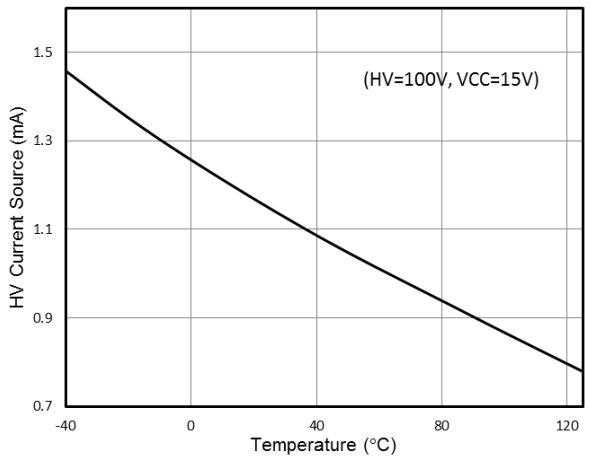


Fig. 1 HV Current Source vs. Temperature

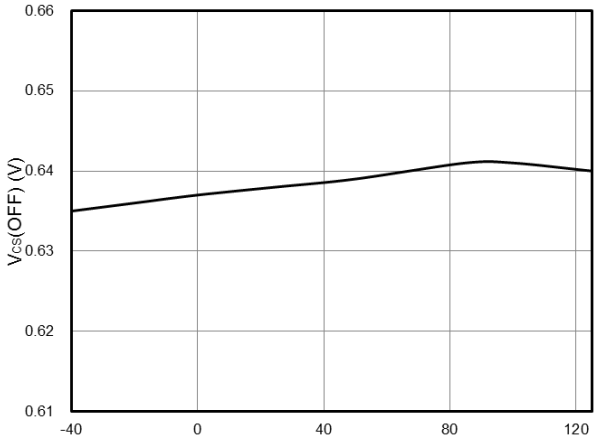


Fig. 2 Vcs (OFF) vs.Temperature

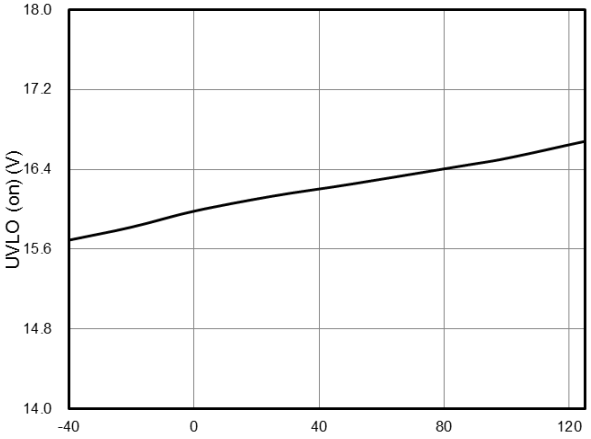


Fig. 3 UVLO (on) v.s.Temperature

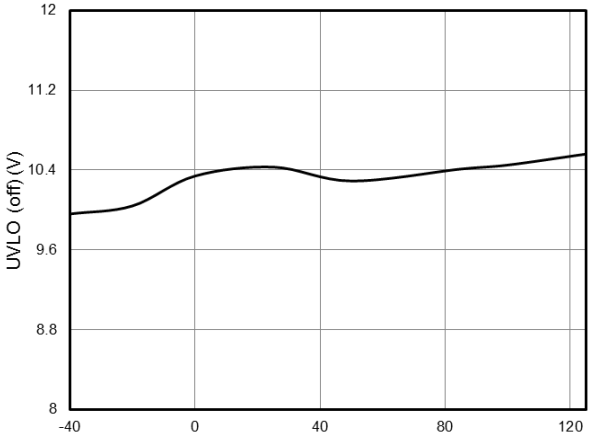


Fig. 4 UVLO (off) vs.Temperature

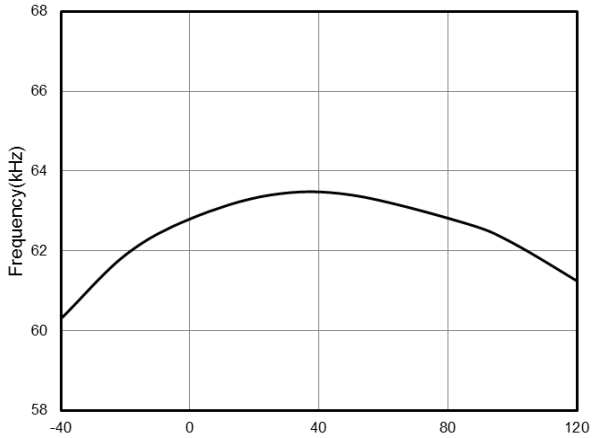


Fig. 5 Frequency vs.Temperature

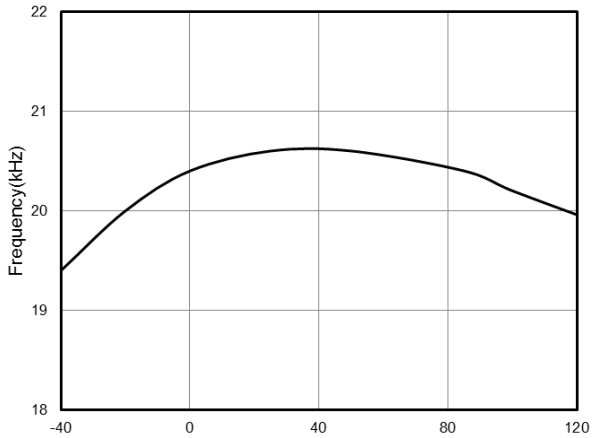


Fig. 6 Green Mode Frequency v.s.Temperature

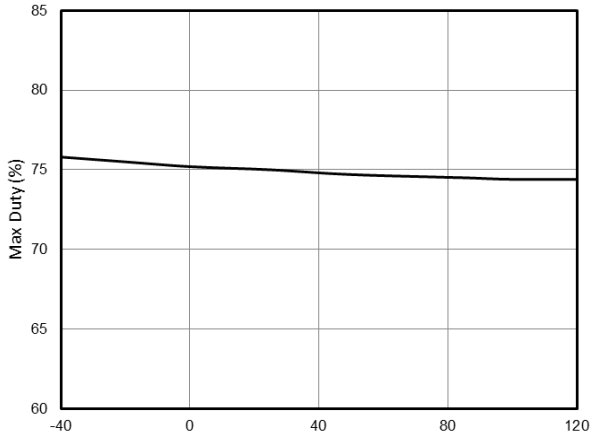


Fig. 7 Max Duty vs. Temperature

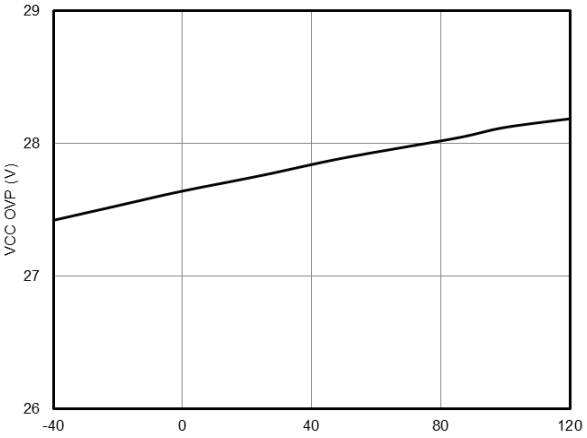


Fig. 8 VCC OVP vs. Temperature

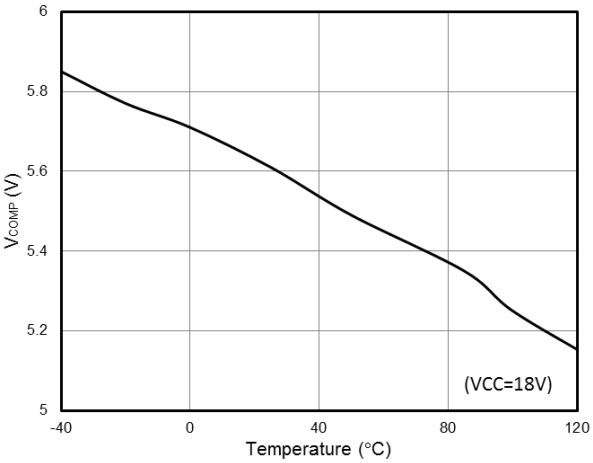


Fig. 9 COMP Open Loop Voltage vs. Temperarure

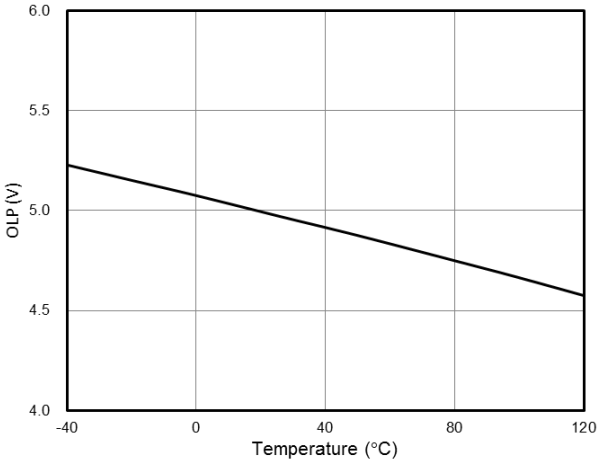


Fig. 10 OLP-Trig Level vs. Temperature

Application Information

Operation Overview

As long as the green power requirement becomes a trend and the power saving is getting more and more important for the switching power supplies and switching adaptors, the traditional PWM controllers would not afford to support such new requirements. Furthermore, the cost and size limitation force the PWM controllers should be more powerful to integrate with more functions to reduce the external part counts. The LD7580A is designed for such application to provide an easy and cost effective solution. Its detailed features are described as below.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

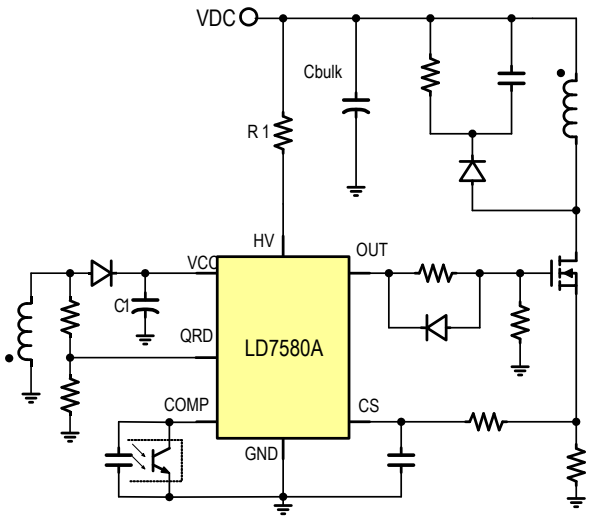


Fig. 11.

Traditional circuits power on the PWM controller through a startup resistor to provide current. However, the startup resistor used here was usually of larger resistance, it therefore required more power and more time to start up.

To achieve the optimized topology, as shown in Fig. 11, the LD7580A was built in with high voltage startup circuit to optimize the power saving. The high-voltage current source will sink current from the bulk capacitor to provide startup current to the PWM IC and charge the Vcc capacitor C1. During startup, the Vcc is below the UVLO(off) threshold thus the current source is activated to supply current of 1mA. Meanwhile, it demands only 300μA for Vcc supply current, so most of the HV current is reserved to charge the Vcc capacitor. By using such configuration, the turn-on delay time will be almost same either in low-line or high-line conditions.

When the Vcc voltage exceeds UVLO(on) level to power on the LD7580A and further to issue the gate drive signal, the high-voltage current source will be disabled and the auxiliary winding of the transformer will take over to supply the current. Therefore, the power loss on the startup circuit can be reduced and it easily achieve power saving. In general application, a 39KΩ resistor is still recommended to place in high voltage path to limit the current if there is a negative voltage applied in any case.

An UVLO comparator is included to detect the voltage on the V_{CC} pin to ensure the supply voltage enough to power on the LD7580A PWM controller and in addition to drive the power MOSFET. As shown in Fig. 12 and Fig. 13, a Hysteresis is provided to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16V and 10.0V, respectively.

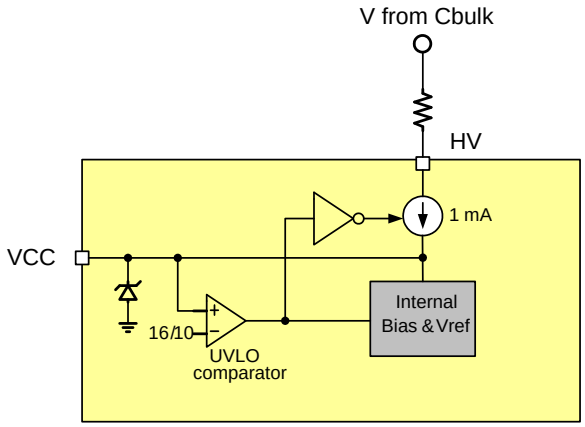


Fig. 12.

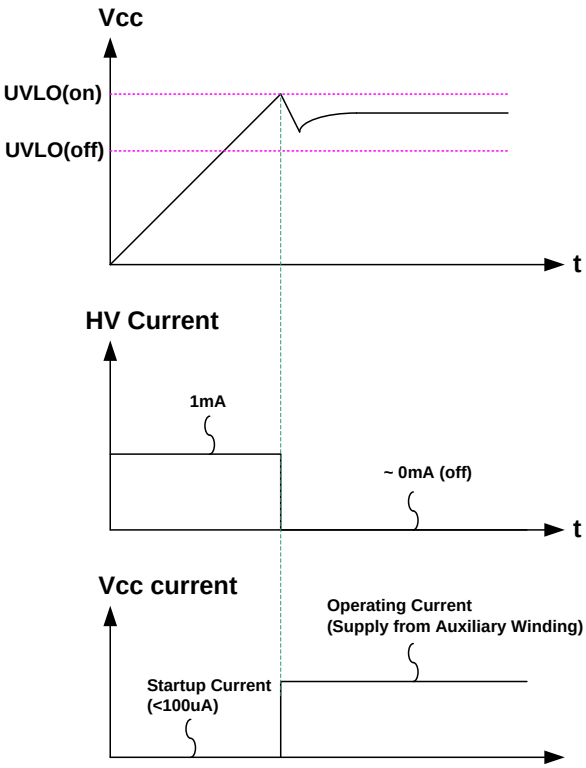


Fig. 13.

Current Sensing, Leading-edge Blanking and the Negative Spike on CS Pin

The typical current mode PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve voltage regulation. The LD7580A detects the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set as 0.85V. Thus the MOSFET peak current can be calculated as:

$$I_{PEAK\,(MAX)} = \frac{0.85V}{R_S}$$

A 200nS leading-edge blanking (LEB) time is incorporated in the input of CS pin to prevent the false-trigger being caused by the current spike. In the low power application, if the total pulse width of the turn-on spikes is less than 200nS and the negative spike on the CS pin is not over -0.3V, the R-C filter (as shown in Fig. 14) is eliminable.

However, the total pulse width of the turn-on spike is determined by the output power, circuit design and PCB layout. It is strongly recommended to add a small R-C filter (as shown in Fig. 15) for higher power application to avoid the CS pin from damage by the negative turn-on spike.

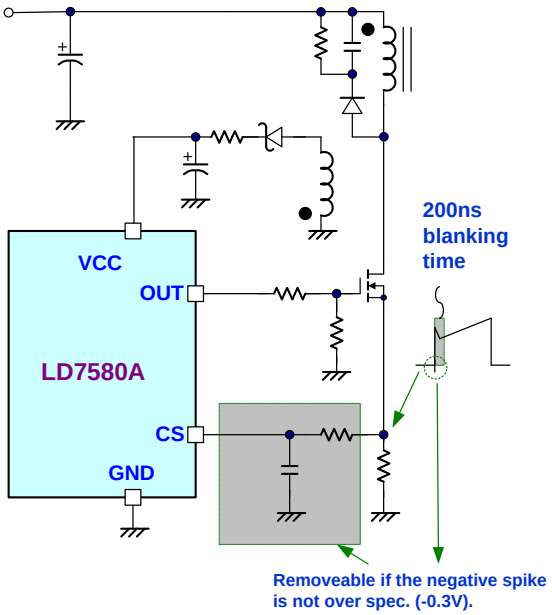


Fig. 14.

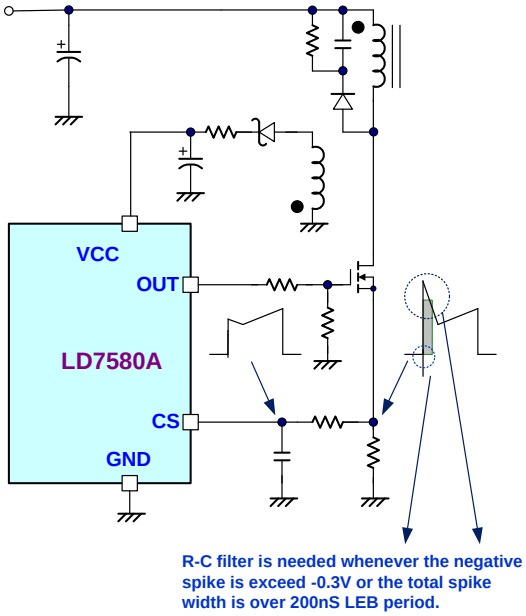


Fig. 15.

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 500mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD7580A is limited to 75% in order to avoid the transformer flux saturation.

Voltage Feedback Loop

The voltage feedback signal is issued from the TL431 in the secondary side through the photo-coupler to the FB pin of LD7580A. The input stage of LD7580A, like the UC384X, is with 2 diodes voltage offset then feeding into the voltage divider with 1/3 ratio, that is,

$$V_{+(PWM\,COMPARATOR)} = \frac{1}{3} \times (V_{COMP} - 2V_F)$$

A pull-high resistor is embedded internally thus can be eliminated on the external circuit.

Oscillator and Switching Frequency

As LD7580A controller is powered on by Vcc, there are four operation modes in estimated load level. At light load (V_{COMP} less than 1.75V), the switching frequency of power supply fixes at 20KHz to reduce switching loss and avoid audio noise.

The switching frequency of LD7580A is various in green mode operation when COMP pin voltage is between 1.75V and 2.35V. Larger COMP voltage produces higher switching frequency.

The LD7580A controller operates in quasi-resonant mode when COMP pin voltage level exceeds 2.35V. In this operation mode, switching frequency is also various as output load changes and mains voltage regulates.

Quasi-Resonant Operation and EMI Performance

The LD7580A is implemented with quasi-resonant operation function. It enables the power supply designers to minimize the EMI components and system cost. Due to valley switching of power MOSFET, MOSFET switching loss and EMI level is reducible.

On/Off Control

If COMP pin is pulled below 1.2V, it will turn off the LD7580A and disable its gate output pin immediately. The off-mode will be released soon after the pull-low signal is removed.

Dual-Oscillator Green-Mode Operation

There are lots of topologies implemented in different chips for the green-mode or power saving requirements such as “burst-mode control”, “skipping-cycle mode”, “variable off-time control “…etc. The basic operation theory of all these approaches intended to reduce the switching cycles under light-load or no-load condition either by skipping some switching pulses or reduce the switching frequency. What LD7580A uses to implement the power-saving operation is Leadtrend Technology’s own IP. By using this dual-oscillator control, the burst -mode frequency can be well controlled and further to avoid the generation of audible noise.

Over Load Protection (OLP)

To protect the circuit from damage at over load or short condition, a smart OLP function is built in with the LD7580A for it, as shown in Fig. 16. Fig. 17 shows the waveforms of the OLP operation. Under such fault condition, the feedback system will force the voltage loop enter toward saturation (6V) and then pull COMP pin voltage to high level. As soon as V_{COMP} trips the OLP threshold of 5.0V and continues for over 60mS, the protection will be activated and then turns off the gate output to stop the switching of power circuit. The 60mS delay time is to prevent the false triggering in the transient of power-on and turn-off.

A divide-2 counter is implemented to reduce the input average power under OLP behavior. As OLP is activated, the output will be latched off and the divide-2 counter will start to count the numbers of UVLO(off). The latch will be released if the 2nd UVLO(off) point is counted then the output is recovered to switch again.

By using such protection mechanism, the average input power can be reduced to extremely low level so that the component temperature and stress can be controlled within the safe operating area.

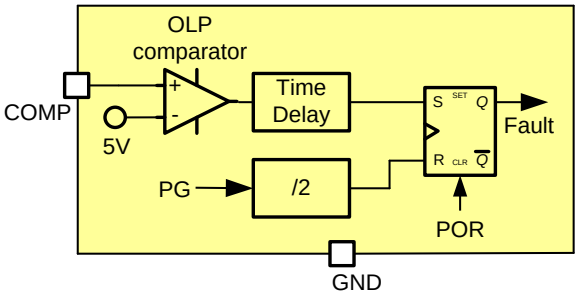


Fig. 16.

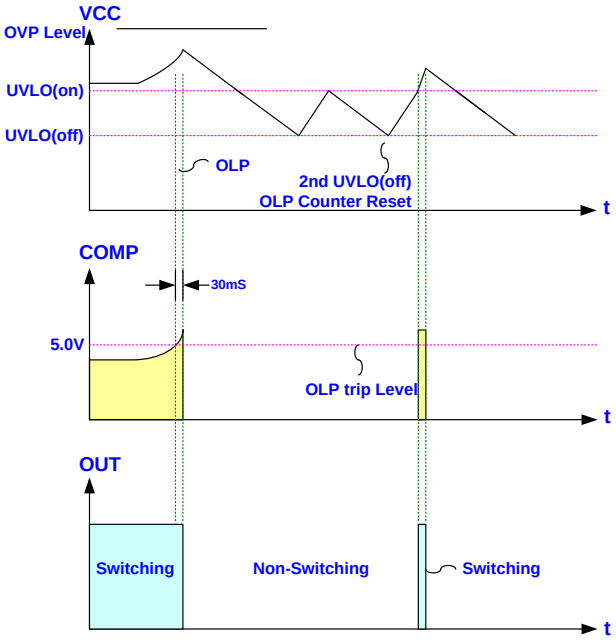


Fig. 17.

OVP (Over Voltage Protection) on Vcc

The V_{GS} ratings of the nowadays power MOSFETs are mostly with 30V maximum. To prevent from V_{GS} fault, LD7580A is implemented with over-voltage protection on Vcc. If Vcc voltage exceeds OVP threshold, the output gate drive circuit will be shutdown simultaneously, thus to stop the switching of the power MOSFET until the next UVLO($_{ON}$) arrives.

The Vcc OVP function in LD7580A is an auto-recovery type protection. If the OVP condition is not released, which is usually caused by the feedback loop open, the Vcc will tripped the OVP level again and re-shutdown the output. The Vcc works in hiccup mode. Fig. 18 shows its operation.

On the other hand, if the OVP condition is removed, the Vcc level will resume to normal level and the output will automatically return to the normal operation.

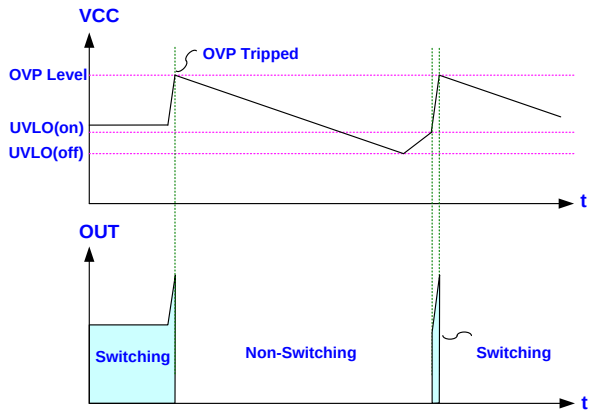


Fig. 18.

Zero Voltage Detection and Q-R Mode Operation

The transformer will be demagnetized after the main power MOSFET turns off. A quasi resonant signal will be detected from auxiliary winding by QRD pin through the external resister.

As soon as the current of the secondary side freewheeling diode falls down to zero during MOSFET-off period, the transformer's core has been demagnetized completely. V_{DS} of MOSFET will resonate in discontinuous current mode. The resonance frequency (F_{QR}) will be obtained as below.

$$F_{QR} = \frac{1}{2\pi\sqrt{L_m * C_R}} (HZ)$$

L_M = Inductance of primary winding

C_R = Resonance equivalent parasitic capacitance

If V_{DS} voltage falls from max plateau value to resonant valley level, it will trip QRD comparator as QRD pin voltage is approaching 55mV. The LD7580A will turn on MOSFET after first valley voltage is in resonant period.

The over voltage protection is built in QRD pin. It will sample the plateau voltage after power MOS turns off. The delay time (1.6μS Typ.) of OVP guarantees a clean plateau, providing a leakage inductance ringing that has been fully damped.

Pull-Low Resistor on the Gate Pin of MOSFET

An anti-floating resistor is implemented in the OUT pin to prevent any uncertain output from MOSFET working abnormally or false triggering-on. However, such design won't cover all the conditions of disconnection of gate resistor R_G. It is still strongly recommended to have a resistor connected at the MOSFET gate terminal (as shown in Fig. 19) to provide extra protection for fault condition.

This external pull-low resistor is to prevent the MOSFET from damage during power-on, if the gate resistor is disconnected. So, as shown in Fig. 20, the resistor R8 can provide a discharge path to avoid the MOSFET from being false-triggered by the current through the gate-to-drain capacitor C_{GD}. Therefore, the gate-source of MOSFET should be pulled low and maintain in off-state no matter the gate resistor is disconnected nor opened in any case.

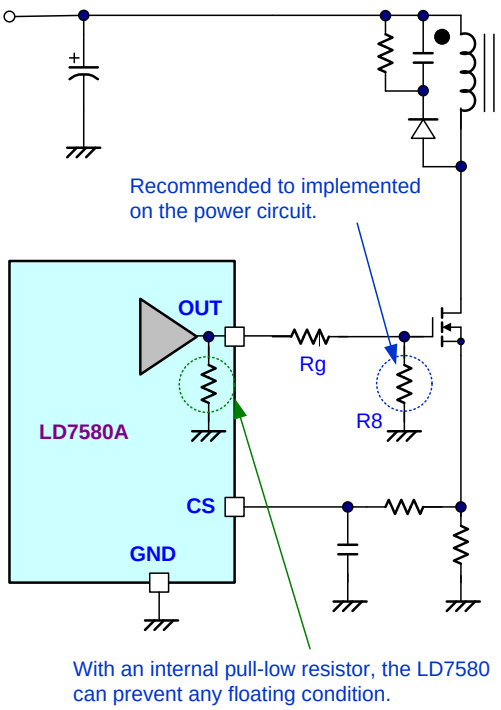


Fig. 19.

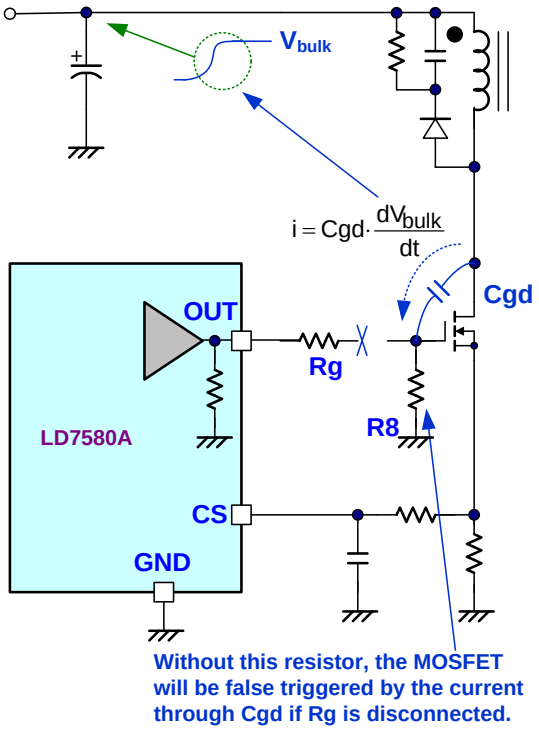


Fig. 20.

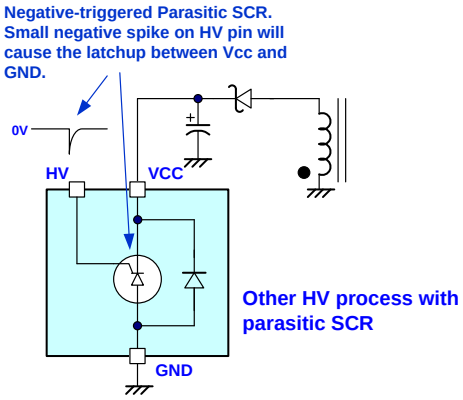


Fig. 21.

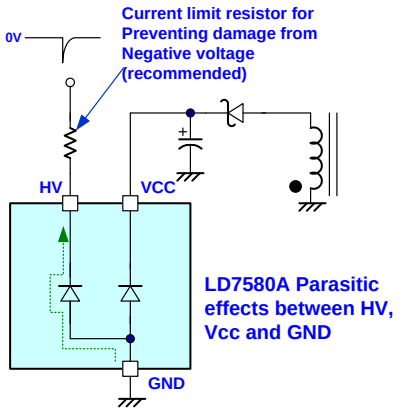


Fig. 22.

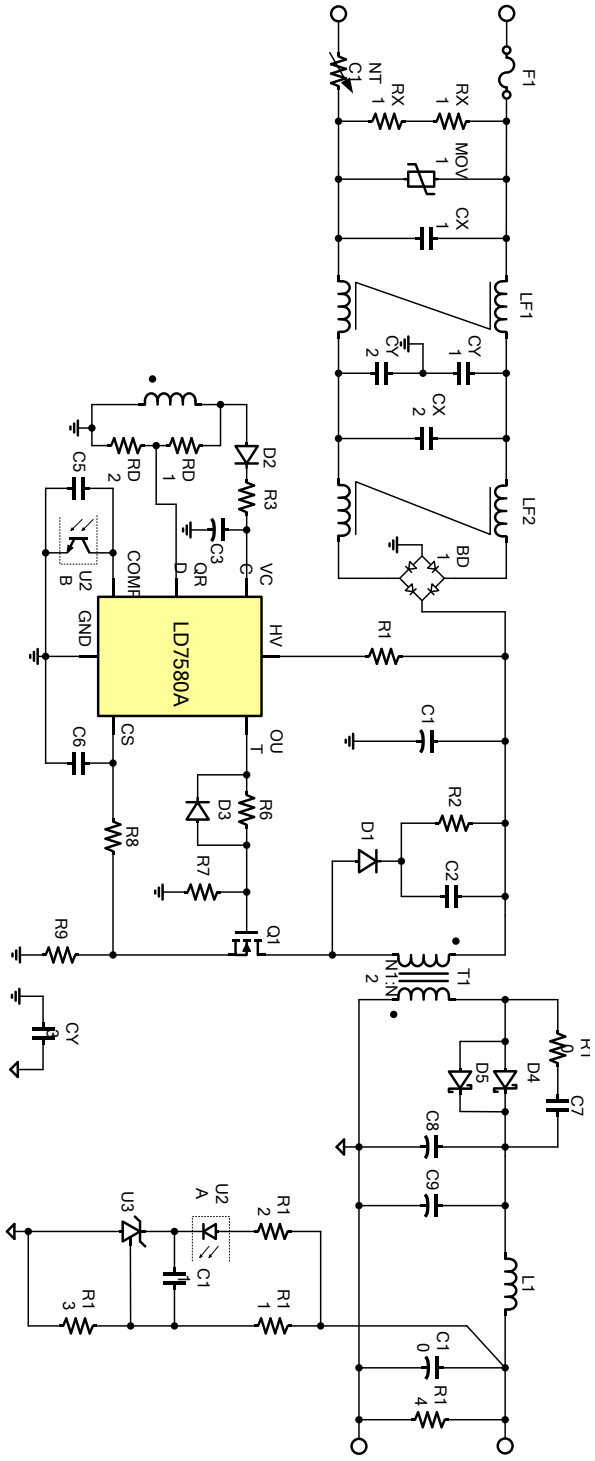
Protection Resistor on the Hi-V Path

In some other Hi-V processes and designs, there is probably some parasitic SCR caused around HV pin, V_{CC} and GND. As shown in Fig. 21, a small negative spike in the HV pin may trigger this parasitic SCR and cause latchup between V_{CC} and GND. It will damage the chip easily since the equivalent short-circuit will be induced by such behavior.

With LD7580A, the designer can eliminate the parasitic SCR efficiently. Fig. 22 shows the equivalent circuit of LD7580A's Hi-V structure. It's capable to sustain negative voltage and superior than similar products. Even though, a 40KΩ resistor is still recommended to be placed on the Hi-V path to act as a current limit resistor if there is a negative voltage applying.

Reference Application Circuit --- 50W (12V/4A) Adapter

Pin < 0.3W when P_{OUT} = 0W & V_{IN} = 264V_{AC}



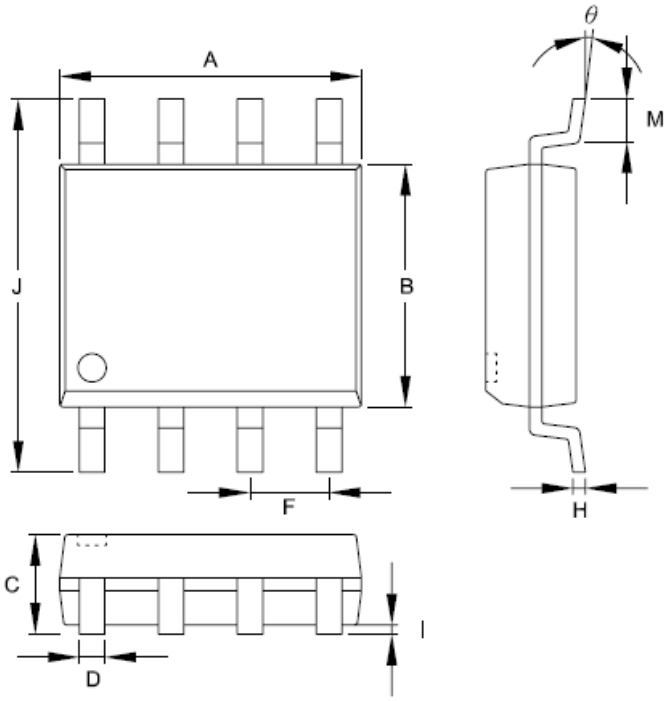
BOM

P/N	Component Value	Note
F1	T3.15A/250V	
NTC	5 Ω/3A	
MOV1	471KD07	
CX1	X2 0.1μF/250V	
LF1	T9*6*3 0.5mH	
LF2	UU15.7 30mH	
CX2	X2 0.33uF/250V	
CY1	Y2 1000P/250V	
CY2	Y2 1000P/250V	
CY3	Y1 1000P/250V	
BD1	2A/600V	
U1	LD7580A	
U2	LTV817C	
U3	TL431AC 2.5V 1%	
R1	51K 1206 5%	
R2	75K/1W 5%	
R3	10 1206 5%	
RX1	1M 1206 5%	
RX2	1M 1206 5%	
R6	100 0805 5%	
R7	10K 0805 5%	
R8	510 0805 5%	
R9	0.82/1W 5%	Ref. Value
RD1	27K 0805 5%	
RD2	27K 0805 5%	

P/N	Component Value	Note
R10	10/1W 5%	
R11	4.7K 0805 1%	
R12	510 0805 5%	
R13	1.2K 0805 1%	
R14	NC	
C1	100μF/400v	
C2	2200PF/1KV	
C3	22μF/50V	
C4	NC	
C5	0.1μF/25V 0805 10%	
C6	100PF/50V 0805 10%	
C7	2200PF/500V 1206 10%	
C8	1000UF/25V	
C9	1000μF/25V	
C10	100μF/25V	
C11	0.1μF/25V 0805 10%	
D1	PR1007 1A/1KV	
D2	PR1002 1A/200V	
D3	LL4148 SOD-80	
D4	20A/100V TO-220	
D5	NC	
T1	PQ2620 PC44	
Q1	7A/600V TO-220	
L1	R3*15 1.5μH	

Package Information

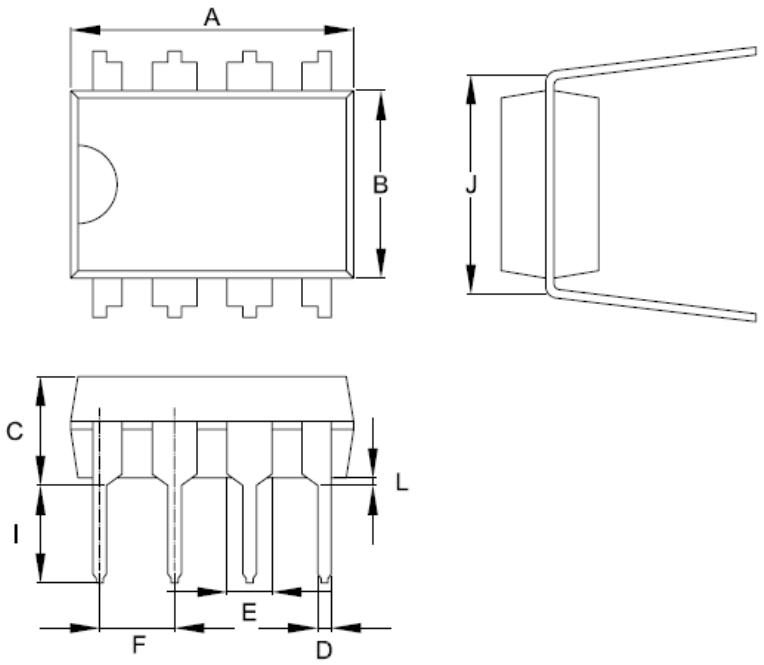
SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	9/5/2012	Original specification.